SPECIFICATION AMENDMENTS

Replace the first paragraph of the application with the following:

This Application is a continuation of U.S. Patent Application No. 09/904,631, filed July 13, 2001, and entitled "Tunable Ferro-Electric Filter", now U.S. Patent No. _____. This application also claims the benefit of U.S. Provisional Application No. 60/283,093, filed April 11, 2001, and entitled "Low Loss Tunable Ferro-Electric Device and Method of Characterization", which is hereby incorporated by reference.

Replace the paragraph including the informality at page 47, ln.3 with this paragraph:

> The formation of a "pedestal" on <u>which</u> ~~shich~~ the f-e capacitors can be optimally integrated as shown in Fig. 11a for a TCC structure using coaxial resonators as an example. The f-e capacitors are integrated as extensions of the input and output capacitors 315a and 315b in Fig. 11a on the pedestal. Alternatively, the f-e capacitors can be patterned and fabricated on the open ends (faces) (not shown) of the coaxial or monoblock resonators.

Replace the paragraph including the informality at page 49, ln.9 with this paragraph:

> Turning now to Fig. 7, a planar realization 150 of the bandpass filter 140 is illustrated. Resonator 102 is formed by a microstrip line 152 grounded through via 154. Note that microstrip line 152 could also be terminated in a suitable lossless ground plane (not illustrated), obviating the need for via 154. Capacitors 153 and 155 are formed by gaps between the input and output microstrip lines 156 and 158 and the resonator microstrip line 152. It is desirable to make the capacitance of capacitors <u>153 and 155</u> ~~155 and 157~~ as large as practical (approximately 0.25 pF) to maximize input and output coupling while still maintaining a planar structure. The microstrip lines are formed on substrate 157 of 99.5% pure alumina, MgO, or sapphire that is preferably of thickness approximately 1.0 mm for providing a maximum microstrip resonator Q. The f-e capacitor 104 is formed as a gap capacitor by pad 160 and mircrostrip line 152, with f-e layer 162 underneath pad 160 and microstrip line 152.